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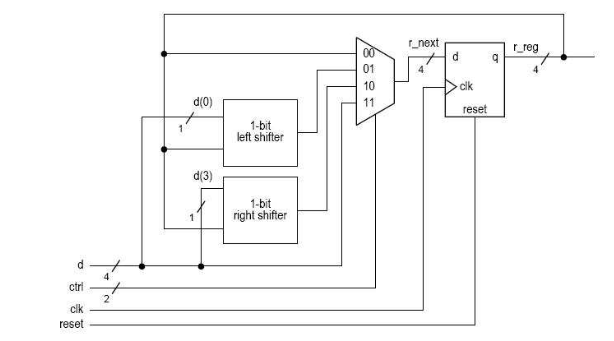
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**EGCP 446**

**In-class assignment Verilog modeling (sequential design)**

1. Design the universal shift register as shown in the figure below. The design will have clk, reset, ctrl (2 bits), d (4 bits) as inputs and q (4 bits as output). r\_next and r\_reg are 4-bit registers for the next state and a present state resp. (You need to define r\_next and r\_reg as reg).
   * Consider the size of data 4 bits.
   * When ctrl = 00, r\_next = r\_reg (no change/no operation)
   * When ctrl = 01, perform shift left operation
   * When ctrl = 10, perform shift right operation
   * When ctrl = 11, load the data from input d (use case statement to select the operations).



In the report, include the Verilog code, testbench and working simulation waveform. You can use the same d and perform all four operations. (When writing a testbench, make sure to load the data first, making ctrl = “11”).